Second generation current conveyors (CCII) Design and Characteristics

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Abstract

Second generation current conveyors (CCII) based topologies presented in the literature have been studied in order to improve performance. This work goes through the design flow of CCII topology, some circuit solutions also presented, to reach low voltage (LV) low power (LP) CCIIs. To improve current linearity between x and z nodes, the self cascode techniques has used to construct topology of CCII with good accuracy.

Keywords: *Current Conveyors, Self cascode, Composite transistor.*

1. Introduction

In current mode architecture, the CCII can be considered the basic building block because all the active devices can be made of suitable connection of one or two CCIIs. This work goes through the design flow of CCII based current mirror topology explaining strategy of CCII design, started with basic level technique to reduce power consumption and in the same time keeping or improving the circuit performance. Next, self cascode technologies in low voltage CMOS design studied to design CCII. Second generation current conveyors (CCIIs) working at low supply voltage with reduced power consumption (in the µW range) and high accuracy are investigated and simulated.

2. Current Mirror based CCII

Traditional n-MOS current mirror shown in Figure 1 [1] can be seen as a CCII.

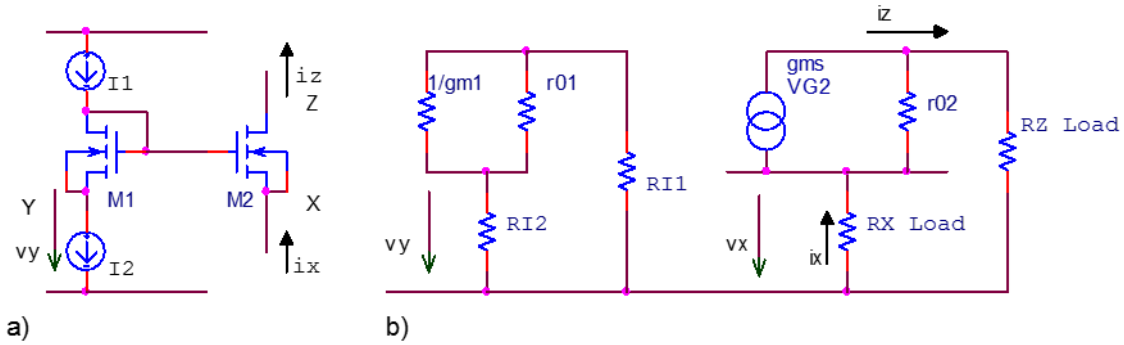


Figure 1. a nMOS current mirror. **b** small signal equivalent circuit.

Considering the circuit depicted in Figure 1, the VG2 determined as a function of the VY:

$$v_{G2} = \frac{R_{I1}}{R_{I1} + \frac{r_{01}}{1 + g_{m1} r_{01}}} v_Y \cong v_Y \qquad 1$$

At X node VX can be expressed as a function of the voltage at M2 gate and VG2=VY:

$$A_v = \frac{v_X}{v_Y} = \frac{g_{m2} r_{02} R_X}{1 + g_{m2} r_{02} R_X} \cong 1 \qquad 2$$

IX and IZ currents are equal, as cleared from the small signal equivalent circuit Figure 1:

$$A_i = \frac{i_Z}{i_X} = 1 \qquad 3$$

Impedance at Y node is given by:

$$r_Y = R_{I2} // \left(\frac{1}{g_{m1}} + R_{I1} \right) \qquad 4$$

X node impedance is affected by the load connected to Z node, while the impedance seen at Z terminal is related to the load connected to X node. X and Z impedances as following:

$$r_x \cong \frac{r_{02} + R_z}{1 + g_{m2} r_{02}} \cong \frac{1}{g_{m2}} \qquad 5$$

If $r_{02} >> R_Z$

$$r_z \cong r_{02} + \left(1 + g_m r_{02}\right) R_x \qquad 6$$

In Figure 2a negative CCII has been implemented, it is possible to add a current mirror as pictured in Figure 2b, Ix and Iz flow in the same direction performing the CCII+ operation

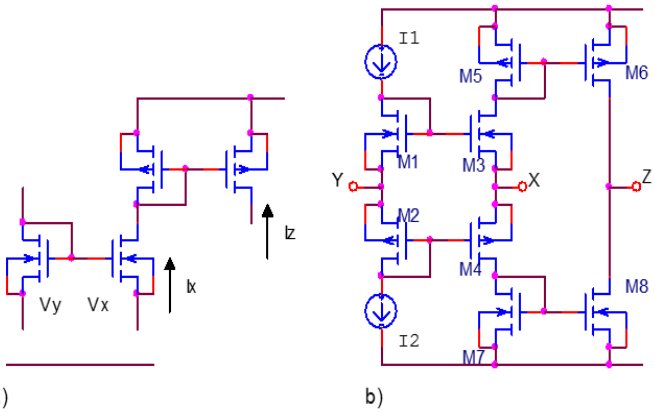


Figure 2 a) Current mirror used for **b)** Class AB CCII based on positive CCII implementation. current mirrors.

The topology presented in Figure 2a can be doubled to obtain a class AB current conveyor, shown in Figure 2b. in this circuit, obviously, I1 and I2 have to be equal [2]-[3]. The input voltage VY is transferred to the output voltage VX of the follower precisely by considering the product gm.ro much greater than 1, the voltage characteristic is very close to the ideal one:

$$A_v = \frac{v_y}{v_x} = 1 + \frac{1}{\left(g_{m3} + g_{m4}\right)\left(r_{o3} r_{o4}\right)} \cong 1 \qquad 7$$

The current mirrors (M5-M6) and (M7-M8) are transferring the current from the X terminals of the current conveyors to their Z terminals. In this case, the quiescent current in all the branches is set by aspect ratios as expressed:

If $g_{m5}=g_{m7}$ and $g_{m6}=g_{m8}$

$$A_i = \frac{i_z}{i_x} \cong \frac{g_{m3} g_{m6} g_{m7} + g_{m4} g_{m5} g_{m8}}{g_{m5} g_{m6} \left(g_{m3} + g_{m4}\right)} = 1$$

or

$$A_i = \frac{i_z}{i_x} = \frac{\left(\frac{W}{L}\right)_6}{\left(\frac{W}{L}\right)_5} = \frac{\left(\frac{W}{L}\right)_8}{\left(\frac{W}{L}\right)_7} \qquad 8$$

If current gain will be set to 1, the circuit will operate as current follower. The input resistance is:

$$r_x \cong \frac{1}{g_{m3} + g_{m4}} \qquad 9$$

The impedance seen at Z node is typically high and given by:

$$r_z \cong \frac{r_{o7} r_{o8}}{r_{o7} + r_{o8}} \qquad 10$$

AB current mirror current conveyor shown in Figure 2b was modified as shown in Figure 3, simulation and the values were summarized in Table 1. The main advantage of this circuit is a wide bandwidth obtained with relatively low biasing currents but has drawback is represented by the limited dynamic range because of:

$$V_{\min} = V_{THP} + V_{THN} + 2V_{DSAT} \qquad 11$$

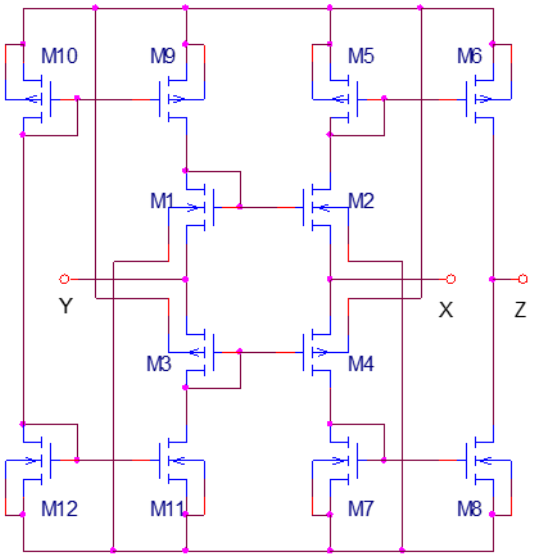
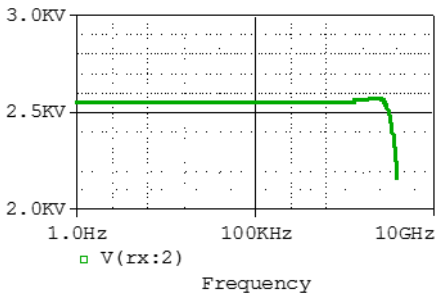


Figure 3 CCII based AB CM

Table 1 CCII based AB CM Characteristic

Data	Value
Voltage Supply	± 2.5 V
Power Consumption	95µW
3dB Bandwidth	200MHz
Dynamic Range	-180mV, +180mV
Node X Parasitic Impedance	2.5 KΩ
Node Z Parasitic Impedance	850kΩ

The following simulation presented in Figure 4 affirming last results.



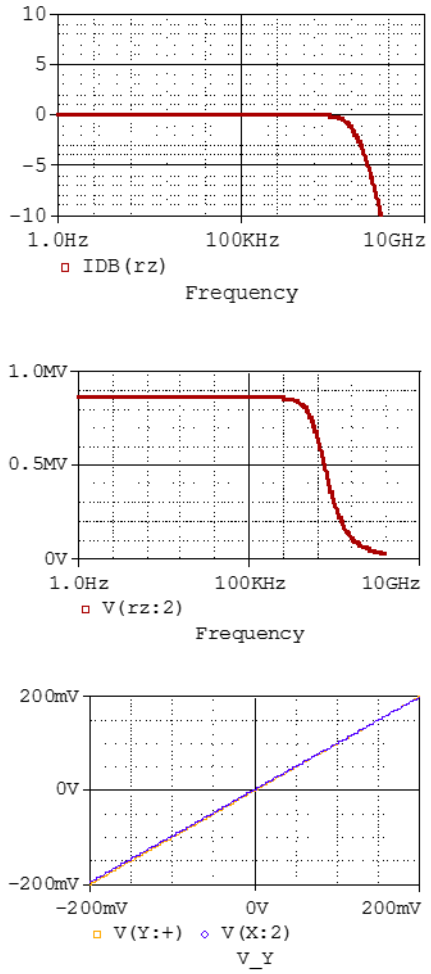


Figure 4: CCII-based CM simulation. a) input resistance rx. b) current transfer ratio iz/ix. c) output resistance rz. d) Y node X node voltages

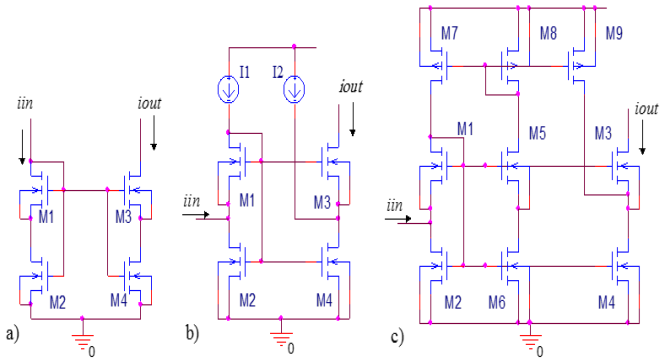


Figure 5 low voltage cascaded current mirror a) self cascode. b) low voltage input. c) high output impedance.

Self cascode current mirror has introduced in [4] as shown in Figure 5a with advantage of high output impedance comparing to the simple one, to reduce input voltage of self cascode current mirrors, low voltage current mirror has been introduced as shown in Figure 5b, the input node is source of M1, instead of its gate. Thus, Vin is no more VT-limited. This is an appreciable feature in low-voltage analog design, since Vin, can be very close to 0V. An implementation of the circuit principle is shown in Figure 5c, where careful design to eliminate current error and achieve Iout=Iin, this current mirror will show output impedance comparable with that of a conventional double cascode current mirror with low voltage input. the aspect ratios have to set as (W/L)2= (W/L)4= m(W/L)6, (W/L)3= (m-1)(W/L)5 =(m-1)(W/L)1 and (W/L)7= W/L)8=(W/L)9, m>1[5].

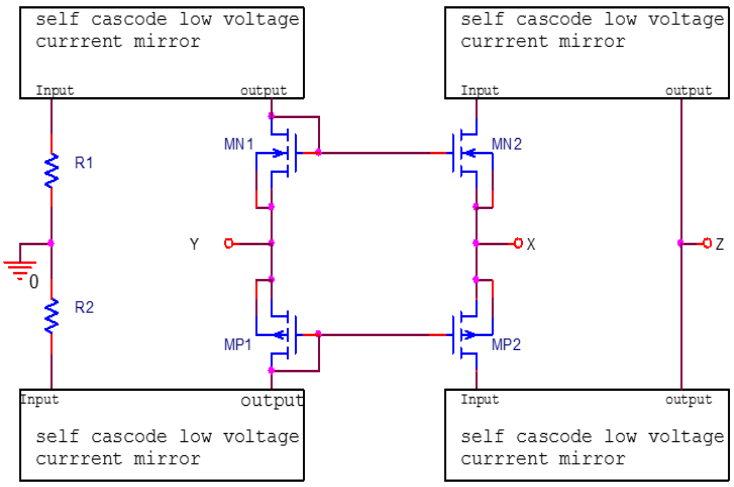
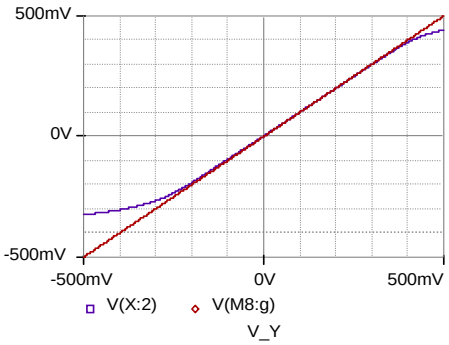
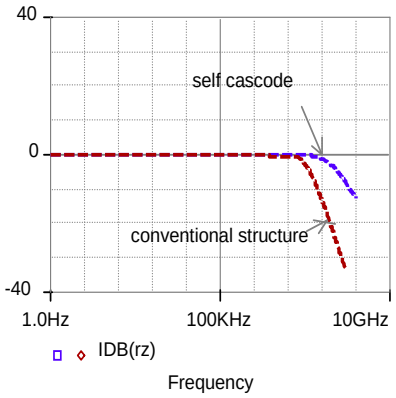


Figure 6 CCII based low voltage self cascode current mirror.

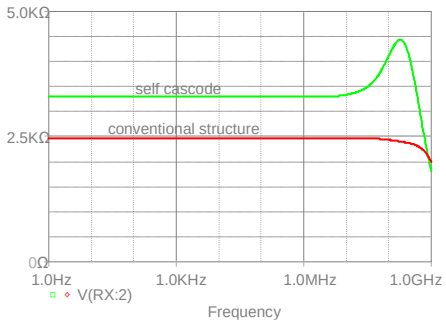
NMOS and PMOS versions of low voltage self cascode current mirrors of Figure 5c employed to construct CM CCII based self cascode current mirrors as shown in Figure 6 [6]. The advantage of self cascode here is that using the advantage of output resistance of composite transistor to get higher output resistance to improve current linearity between x and z nodes and hence minimizing the portion of ix which is lost on output transistors. Figure 7 depicts simulations; the main performance characteristics are summarized in Table 2 which reports a comparison with conventional CCII based current mirrors.



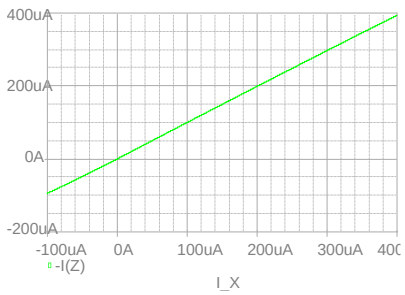
a) Xnode voltage and Ynode.



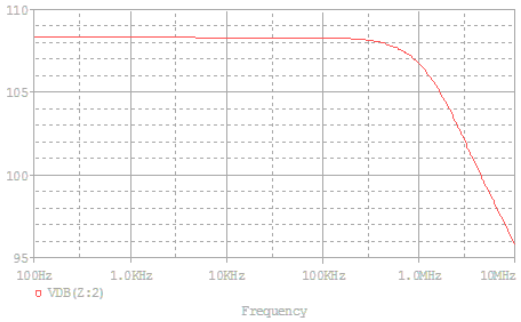
b) Current transfer ratio iz/ix.



c) input impedance rin,x.



d) Ix and Iz linearity.



(e) Output resistance Z normalized in dB.

Figure 7 CCII based low voltage self cascode current mirror characteristics simulation

Table 2 CCII based low voltage self cascode CM charateristics

Characteristics	Composite Transistor CCII	Conventional CCII Based CM
Voltage Supply	±1.5 V	± 1.5 V
Power Consumption	70µW	95 µW
3dB Bandwidth	320 MHz	200 MHz
Dynamic Range	-110 mV, +300 mV	-180 mV, +180 mV
Node X Parasitic Resistance	3.3 KΩ	2.5kΩ
Node Z Parasitic Resistance	2 MΩ	850 KΩ

3. Conclusion

This work has mainly focused on circuit design techniques that would permit the implementation of CCII at low power supply voltages in CMOS technology. The primary limitations of analog circuits at low voltage are a large threshold voltage, large channel length modulation, and poor analog modelling. The last two limitations are caused by short-channel technology. The best solution to the large channel length modulation problem is the composite transistor (self cascode). Self-cascode technique provides wide input and output swing and high current transfer accuracy within a wide current range. The advantages of self-cascode circuits are numerous, and include the ability to implement a low voltage CCII with good performance characteristics. Simulations proved that self cascode current mirrors can be used to build low-voltage high-linearity, high current- efficiency current output stages, these structures are also suitable for low-voltage design of other current-output-based active devices, such as current conveyor based operational amplifiers.

Nomenclature:

g_m :Gate transconductance [S],

Ix : X node current (input current), [A],

Iz : Z node current (input current) [A],

L: Channel length [m],

R: Resistance [Ω],

rx : X node impedance[Ω],

rz: Z node impedance[Ω],

Ry : Y node impedance[Ω],

ro : Output resistance [Ω],

$V_{G:}$ Gate voltage [V],

V_T : Threshold voltage [V],

Vy : Y node voltage (input voltage) [V],

vx : X node voltage [V],

W : Channel width [m].

References

1. A. Sedra, G. W. Roberts. “Current-conveyor theory and practice”, analogue IC design: The current mode approach. Peter peregrinus, London, 1990.

2. Fabre, A., and Alami, M. “A precise macromodel for second generation current-conveyors”, IEEE Trans. Circuits and System, (1997), pp. 639–642.

3. C. Toumazou, F. J. Lidgey and C.A. Makris, “Extending Voltage-Mode Op-amps to Current-Mode Performance”, IEE Proc.Pt. G, 137 (2), pp. 116-130, 1990.

4. Galup-Montoro, C., Schneider, M. C. and Loss, I. J. B. “Series-Parallel association of FET’s for high gain and

high frequency applications", IEEE J. Solid-state Circuits, vol. 29, no. 9, 1994, pp. 1094-1101.

5. G. Palmisano, G. Palumbo, S. Pennisi, "High linearity CMOS current output stage", Electronics Letters, 31, 1995, pp. 789-790.
6. I. Eldbib, J. Brzobohaty, "Low voltage current conveyor techniques", Proceeding of 14th conference EEICT 2008, vol. 4, pp. 348-352.